



**Altera Nios[®] II Embedded Processor
Design Contest 2007
South Asia/Pacific Region**

(India, Australia/New Zealand, Singapore/ Malaysia/ Thailand)

Entry Registration Form

Deadline of Submission April 30th, 2007

Name(English)	
Correspondence Address	
Contact Telephone No.	
Mobile Phone No.	
Email Address	
Name of University/Institution	
Name of Advisor	
Contact Telephone No. of Advisor	
Email Address of Advisor	
<p>I/We have received a copy of the contest guidelines and agree to abide by them. I/We understand that Altera is under no obligations to exercise any or all of the rights, licenses, and privileges herein granted. Participant hereby releases and discharges Altera and the contest sponsors from any and all liability arising out of participation in the contest. I/We agree that any work submitted as part of my/our participation in this contest will be the original work of the participant(s) named herein. I/we agree to execute a Participant Release Form as a condition of my/our participation in this contest.</p>	
Signature of Applicant 1	Date
Signature of Applicant 2	Date
Signature of Applicant 3	Date
Signature of Advisor	Date

Altera Nios® II Embedded Processor Design Contest 2007 – South Asia/Pacific Region

(Australia, India, Malaysia, New Zealand, Singapore, Thailand)

Submission & Evaluation Guidelines

Submission Deadline: All designs should be submitted on or before September 15th 2007

Deliverables: Design Contest participants are required to submit the following:

1. Final project paper according to the template specified by Altera. This template will be used for ease of evaluation. Please refer to the attachment that shows the required template.
2. Compilation report file and simulation waveforms showing correct functionality of the design. Altera may ask for more details on the design such as RTL simulation results etc if required.
3. In-system demonstrations of the design that shows correct hardware functionality of the designs. An expert from Altera / Achieva / Braemac will oversee such demonstrations.

Note: The project papers submitted for this contest will be compiled and published by Altera in a book. Each team participating in the contest will receive one complimentary copy of this book.

Altera reserves the right to edit project papers prior to publication to ensure compliance with Altera's publication guidelines. Altera also reserves the right to withhold project papers from publication for any reason.

IMPORTANT: Each individual participant in this contest will be required to sign a Participant Release and Copyright Transfer Form, which is to be posted to the contest website.

By signing this release form, you certify that the project papers and supporting materials you submit and display during this contest are your original work and that you are not infringing any third party intellectual property rights. By signing this release form, you will also transfer the copyright ownership of your project papers and supporting materials to Altera. You and the other members of your project team will retain the right to reproduce, distribute, and create derivative works of your project papers and all supporting materials.

Evaluation Methodology:

1. The designs will be scored by a panel of experts from Altera /Achieva/ Braemac.
2. The score will be calculated based on the scoring guidelines mentioned in Table 1
3. The design receiving the highest score will be declared the 1st prize winner. There will also be one 2nd and one 3rd prize for the designs receiving the 2nd highest and the 3rd highest scores.

Table 1: Scoring Guidelines for Nios Design Contest

Design Phase	Category	Score	Examples
Design Concept	Complexity	5 pts	-Design uses RTOS or -Multiple Nios cores sharing and inter-core communications
		4 pts	- Uses DSP Algorithm or - Does packet processing or - Does graphic acceleration
		3 pts	- greater than 70% LE /memory utilization or - uses complex IP cores
		2 pts	- uses two masters on Avalon bus
		1 pts	- greater than 50% LE / memory utilization
		0 pt	- None of the above
		Functionality	5 pts

		4 pts	- custom instruction or - custom peripheral for hardware acceleration
		3 pts	- custom peripheral without hardware acceleration
		2 pts	- More than 8 peripherals on SoPC bus
		1 pts	- More than 5 peripherals on SoPC bus
		0 pts	- None of the above
Design Implementation	Completeness	5 pts	- Final report + 100% software complete + 100% hardware demonstration
		4 pts	- Final report + 100% software + 80% hardware demonstration
		3 pts	- Final report + software debugging AND hardware debugging
		2 pts	- Final report + software debugging
		1 pts	- Final report + hardware debugging only
		0 pts	- None of the above
Documentation	Completeness	5 pts	- Complete all 7 parts in proper format with proper illustrations and full documentation of the final project.
		4 pts	- Complete all 7 parts in proper format
		3 pts	- Complete mandatory parts + detailed design description + design features
		2 pts	- Complete mandatory parts + detailed design description
		1 pts	- Complete all mandatory parts (Design Introduction, Function Description, Performance Parameters, and Design Architecture.
		0 pts	- No submission * *Violation of the contest agreements. The project is said to be disqualified.

Prizes

The following prizes will be awarded for the Altera Nios Design Contest –*Australia, India, Malaysia, New Zealand, Singapore, Thailand*

- 1st Prize – US \$1500
- 2nd Prize – US \$1000
- 3rd Prize – US \$500
- Star Award (Australia/New Zealand) – US\$250
- Star Award (Singapore/ Malaysia/ Thailand) – US\$250

In addition, we will be also giving a Best Instructor Award to the professor who has shown exemplary teaching skills with the Nios II embedded processor.

Awards Ceremony

The prizes for the Nios Design Contest will be given away at the Awards Presentation Ceremony at the *SoPC World 2007 Conference*. Details of the conference date and venue will be sent later. Altera will also pay for travel expenses for the three award winning teams and the best instructor.

Remarks

Altera, as the sponsor of this contest, will retain the copyright ownership of the project papers and other usufruct of the design and documents of this contest.

Appendix: Final Project Paper Submission Template

* Name of the Design / Project:	
* Name of College/ University/ Institute:	
* Name & Details of the Students & Instructor	
Notice	<ol style="list-style-type: none"> 1) Please send this paper to rmohamme@altera.com before September 15th 2006 2) Altera, the sponsor of the contest, holds the copyright and the usufruct of all the designs and their documents of this contest. 3) The parts with "*" are required to be completed. And please hand over the others with your substantial design. 4) Each team member (students and instructor) should sign and return the Participant Release and Copyright Transfer Form.
<p>PART I * Design Introduction (mandatory): (Please give some general information of your design, e.g. purpose of the design, application scope, and targeted users. Please also include a detailed description of why you used Nios soft core processor to do the design.)</p>	
<p>PART I * Function Description (mandatory): (Please give detailed information to show the functionality of your design and how to implement it.)</p>	
<p>PART III * Performance Parameters (mandatory): (Please enumerate some performance parameters that the design needs to reach. If possible, please compare the actual performance realized in your design with the design parameter, and then appraise the function of Nios processor in the design.)</p>	
<p>PART IV * Design Architecture (mandatory): (Please give the system design scheme of your design or both hardware design block diagram and software flow chart.)</p>	

PART V

Design Description:

(Please give the detailed description of the implementation method and steps of the design, especially how the design is implemented using the concept and method of SOPC.)

PART VI

Design Features

(Please enumerate the features of your design. And illuminate how SOPC plays an important role in the design implementation.)

PART VII

What you learned during the design (Conclusion)

(During this contest, you certainly increased your understanding of Nios and made some conclusions. These conclusions will be useful for others who are learning about Nios or using Nios as reference. Please tell us what you learned during the design.)

Altera Nios® II Embedded Processor Design Contest 2007 – South Asia/Pacific Region

(Australia, India, Malaysia, New Zealand, Singapore, Thailand)

Purpose of Activity

- Increase the students' interest on Embedded Processors
- Improve their VLSI design capability and creativity
- Motivate the development of System-on-a-Programmable Chip (SOPC) system design

About Nios II embedded processor

Altera's Nios® II family of soft-core embedded processors is optimized for programmable logic and system-on-a-programmable-chip (SOPC) integration. With three Nios II cores and multiple FPGA device families to choose from, developers can accommodate a wide range of performance and price points, achieving performance over 200 DMIPs in Stratix® II FPGAs, and costs as low as \$0.35 in Cyclone™ II devices. Nios II cores are general-purpose RISC processors that can be combined with user logic and programmed into an Altera® FPGA. The processor features a 32-bit instruction set, 32-bit data path, and configurable instruction and data caches. Nios II embedded processors are royalty free when used in Altera FPGAs and HardCopy® devices. For more information, visit www.altera.com/nios2.

Eligibility

Graduate or post-graduate students of the institutions in the South Asia/ Pacific region including Australia, New Zealand, India, Singapore, Thailand and Malaysia with sufficient background in basics of VLSI and embedded system design. Applicants should apply as an individual or a team (maximum 3 members in the team).

Registration

Please fill in the contest entry form and fax it back to Braemac at 61 2 95506377 for registration. You can also send an email to Stephen Albuquerque at s.albuquerque@braemac.com.au for registration.

Deadline : April 30 2007.

Training & Support

We will provide training to all the teams who register for the contest. Field Application Engineers from Braemac will be available for design support throughout the contest.

Submission of Abstracts

Deadline for Abstracts: **June 15, 2007**

The project abstract should contain a)Name, b)Name of institution, c)Department, d)Type: Individual/Team (Names of team members), e)Email, f>Contact no, g)Academic supervisor or advisor, an abstract (not more than 300 words), main content, circuit diagram, block diagram and reference (if any). The work should be original in treatment of an engineering concept using Altera Nios and specify the author's contribution to the subject while the concept needs not be original in itself.

Scope of application

1. Communication and Networking
2. Computer & Storage
3. Digital Consumer
4. Industrial and Automotive

Scoring criteria

The scores for the designs will be based on the scoring guidelines mentioned in the attachment.

Technology Level (Select most suitable components to complete the best design)	40%
Creativity (New or improved methodology)	20%
Practical of Mass Production (Suitable for mass production, practical to use)	40%

Judges

Louie Leung, Marketing Director, Asia Pacific, Altera
Steve Groom, Engineer, Braemac
Andrew Soh, Product Marketing Manager, Achieve Singapore
Malhar Deshpande, Asst FAE Manager, Achieva India
Gangatharan Gopal, FAE Manager, South Asia Pacific, Altera

Submission of Final Project

Deadline: September 15 2007

Final evaluation

The results of the design contest will be announced by **October 20, 2007**

Awards*

1 st Place Winner:	US\$1500
2 nd Place Winner:	US\$1000
3 rd Place Winner:	US\$500
Outstanding Academic Supervisor (instructor of 1 st place winner):	US\$500

* Top 3 winning papers will be included in the 2007 Nios Design Contest Book.

Star Award:

Star Australia Award US \$250

This award will be given to the best design from Australia / New Zealand.

If the best design as award winner, the Star Award will be given to the next best design from Australia/New Zealand

Awards Presentation Ceremony

More details on the award ceremony will be communicated to you as they become available. Participating students will also receive a certificate of participation in recognition for their efforts.

Contacts:

Stephen Albuquerque
+61 2 85945629
s.albuquerque@braemac.com.au
Braemac (Sydney)

Organizer:



Co-organizer:

